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09/623,655	09/07/2000	Takafumi Maruyama	43889-977	6288

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Jack Q Lever Jr
McDermott Will & Emery
600 13th Street NW
Washington, DC 20005-3096

EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	5

DATE MAILED: 01/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/623,655	MARUYAMA ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the c ver sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-9,13 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,13 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 September 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *1,3*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Preliminary Amendment filed on 7th of September 2000. Claims 1 and 13 have been amended; claims 3, 10-12 , 15 and 16 have been canceled; and no claim has been newly added. Currently, claims 1, 2, 4-9, 13 and 14 are pending in this application.

Specification

2. The disclosure is objected to because of the following informalities:

On page 2, lines 16-17, substitute "Figure 17(a) and Figure 17(b)" by --Figure 21(a) and Figure 21(b)--.

On page 12, line 24, substitute "an output unit 7b" by --an output unit 7d--.

Appropriate correction is required.

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicants' cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

4. Figures 21(a) and 21(b) should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (See Application, page 2, lines 16-17 and page 10, lines 4-6). See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: the reference sign 5b for the subject matter "the cloak line" on page 14, line 17 is not shown in the drawings. A proposed drawing correction

or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 1, 2, 4-8, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murata [JP 404133154 A; cited by the Applicants] in view of Shibazaki [US 5,809,257 A] and what was well known in the art, as exemplified by Kawagoe [US 6,208,548 B1].

Referring to claim 1, Murata discloses a semiconductor integrated circuit system (i.e., bus switching control system in Fig. 1) having a plurality of units (i.e., bus masters 1a-c and slaves 4a-c in Fig. 1) and making said plurality of units transmit and receive signals to and from each other (See page 362+, the left, lower paragraph [operation]), comprising: a bus selector device (i.e., bus switching circuits 2a-c, bus selecting circuits 3a-c and bus 10b in Fig. 1) connected to said plurality of units via a plurality of buses (i.e., bus 10a and bus 10c in Fig. 1), said bus selector device receiving connection information among said plurality of units (i.e., receiving access information, viz., REQ signal and address data in Fig.

2) and selecting among connections of said plurality of buses in accordance with said connection information (See page 363+, the left, upper paragraph [embodiment]).

Murata does not expressly teach said bus selector device being provided with latch means for holding signals to be transmitted to or received from said plurality of units to adjust timings of signal transmission and reception.

Shibazaki discloses a bus control apparatus for data transfer system (Fig. 7), wherein a bus selector device (i.e., data selector 22 and 23 in Fig. 8) being provided with latch means for holding (i.e., buffer section 20, 25 and data holding section 21, 24 in Fig. 8) signals to be transmitted to or received from a plurality of units (i.e., memories, e.g., MEMORY A and B in Fig. 8) to adjust timings of signal transmission and reception (See col. 7, lines 51-59 and Fig. 9A-F).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said latch means for holding signals (i.e., buffer section and data holding section), as disclosed by Shibazaki, in said bus selector device, as disclosed by Murata, for the advantage of improving the reliability and operability of said semiconductor integrated circuit system (See Shibazaki, col. 4, lines 35-37).

Murata, as modified by Shibazaki, does not expressly teach said plurality of units are a plurality of chips. The Examiner takes Official Notice that said plurality of units are a plurality of chips, such as memory chips, is well known to one of ordinary skill in the art of memory architecture, as evidenced by Kawagoe (See Fig. 1 and col. 4, lines 53+ [Embodiment 1]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have recognized said plurality of units (i.e., bus masters and slaves), as disclosed by Murata, as a plurality of chips (i.e., memory chips), as disclosed by Kawagoe, since it would have the same structure of master-slave relationship among devices for bus communicating application (e.g., memory read/write operations).

Referring to claim 2, Murata teaches said bus selector device (i.e., bus switching circuits 2a-c, bus selecting circuits 3a-c and bus 10b in Fig. 1) comprising switch means for switching (i.e., gates 11-13 in Fig. 3 and gates 15-17 in Fig. 4) among said connections of said plurality of buses (See Fig. 1); and determination means for determining (i.e., address decoder 14 of Fig. 3 and gates G20-G22, FF 26-28 in Fig. 4) said connection information among said plurality of chips received (i.e., received access information, viz., REQ signal and address data in Fig. 2), and for outputting a switch signal (i.e., gate enable signals in Figs. 3 and 4) in accordance with determination results to said switch means (See page 363, the left, upper paragraph, lines 14-18).

Referring to claim 4, Murata teaches said plurality of chips (i.e., bus masters 1a-c and slaves 4a-c in Fig. 1) include at least one master chip (i.e., bus masters 1a-c in Fig. 1) and a plurality of slave chips (i.e., slaves 4a-c in Fig. 1).

Referring to claim 5, Murata teaches said master chip (e.g., bus master 1a of Fig. 1) outputs said connection information among said plurality of chips (i.e., access information, viz., REQ signal and address data in Fig. 2) to said bus selector device (i.e., bus switching circuits 2a-c, bus selecting circuits 3a-c and bus 10b in Fig. 1); and said master chip and said bus selector device are connected to each other (See Fig. 2) with a single bus (i.e., bus 10a-1 of Fig. 2), said single bus carrying said connection information among said plurality of chips (See page 363, the left, upper paragraph, line 19 through the right, lower paragraph, line 1).

Referring to claim 6, Murata teaches said master chip (e.g., bus master 1a of Fig. 1) outputs said connection information among said plurality of chips (i.e., access information, viz., REQ signal and address data in Fig. 2) to said bus selector device (i.e., bus switching circuits 2a-c, bus selecting circuits 3a-c and bus 10b in Fig. 1); and said master chip and said bus selector device are connected to each other (See Fig. 2) with two or more buses (See page 363, the left, upper paragraph, lines 12-14; i.e., wherein in fact that the bus 10a-1, 10b-1-1 ~ 10b-1-3 are consisted of a plurality of signal lines for address, data,

control signal, etc., impliedly suggests that the bus, e.g., bus 10a-1 of Fig. 2, comprises two or more buses, such that address bus, data bus, control signal bus, etc.), one of said two or more buses (i.e., address bus and control signal bus) carrying said connection information among said plurality of chips (i.e., access information).

Referring to claim 7, Murata teaches said two or more buses the bus (e.g., bus 10a-1 of Fig. 2 comprises two or more buses, such that address bus, data bus, control signal bus, etc.) include a command bus (i.e., address bus and control signal bus for REQ signal), said command bus being also used as a connection information bus to carry said connection information among said plurality of chips (i.e., as a bus for transferring access information, viz., REQ signal and address data; See Fig. 2).

Referring to claim 8, Murata teaches said one of said two or more buses (i.e., address bus and control signal bus for REQ signal) to carry said connection information among said plurality of chips (i.e., access information, viz., REQ signal and address data in Fig. 2) is a specifically designed connection information bus (i.e., specifically designed bus carrying address and control signal for REQ signal).

Referring to claim 13, Murata discloses a bus selector device (i.e., bus switching circuits 2a-c, bus selecting circuits 3a-c and bus 10b in Fig. 1) connected to a plurality of units (i.e., bus masters 1a-c and slaves 4a-c in Fig. 1) with a plurality of buses (i.e., bus 10a and bus 10c in Fig. 1) and selecting among connections of said plurality of buses (See page 363+, the left, upper paragraph [embodiment]), comprising: switch means for switching (i.e., gates 11-13 in Fig. 3 and gates 15-17 in Fig. 4) among said connections of said plurality of buses (See Fig. 1); determination means for receiving and determining (i.e., address decoder 14 of Fig. 3 and gates G20-G22, FF 26-28 in Fig. 4) connection information among said plurality of units (i.e., access information, viz., REQ signal and address data in Fig. 2), and for outputting a switch signal (i.e., gate enable signals in Figs. 3 and 4) in accordance with determination results to said switch means (See page 363, the left, upper paragraph, lines 14-18); data input means for receiving data (e.g., means for receiving data through data signal lines within bus 10a-1 in Fig. 1) from

any one of said plurality of units (i.e., bus master 1a of Fig. 1); data output means for outputting said data (e.g., means for outputting said data through data signal lines within bus 10c-1 in Fig. 1) to at least one of said plurality of units (i.e., slave 4a of Fig. 1) via one of said plurality of buses (i.e., bus 10a-1 and bus 10c-1 in Fig. 1) that is selected by switching of said switch means (i.e., selected by gates 11 in Fig. 3 and gate 15 in Fig. 4); and internal buses (i.e., bus 10b in Fig. 1) connected to said plurality of buses (i.e., bus 10a and bus 10c in Fig. 1).

Murata does not teach a plurality of latch means arranged on said plurality of internal buses.

Shibazaki discloses a bus control apparatus for data transfer system (Fig. 7), wherein a plurality of latch means (i.e., buffer section 20, 25 and data holding section 21, 24 in Fig. 8) arranged on a plurality of internal buses (i.e., bus lines 200 and signal lines 201 and 202 in Fig. 7).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said latch means for holding signals (i.e., buffer section and data holding section), as disclosed by Shibazaki, in said bus selector device, as disclosed by Murata, so as to adjust timings of signal transmission and reception (See Shibazaki, col. 7, lines 51-59 and Fig. 9A-F) for the advantage of improving the reliability and operability of said semiconductor integrated circuit system (See Shibazaki, col. 4, lines 35-37).

Murata, as modified by Shibazaki, does not expressly teach said plurality of units are a plurality of chips. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have recognized said plurality of units (i.e., bus masters and slaves) as a plurality of chips (i.e., memory chips), which has been discussed / addressed above in the claim 1.

Referring to claim 14, Murata teaches control signal input means for receiving a control signal (e.g., means for receiving control signal through control signal lines within bus 10a-1 in Fig. 1) from one of said plurality of chips (i.e., bus master 1a of Fig. 1) for another chip (i.e., slave 4a-c in Fig. 1); and control signal output means for outputting said control signal (e.g., means for outputting said control

signal through control signal lines within bus 10c-1 in Fig. 1) to at least one of said plurality of chips (i.e., slave 4a of Fig. 1) through one of said plurality of buses (i.e., bus 10a-1 and bus 10c-1 in Fig. 1) selected by switching of said switch means (i.e., selected by gates 11 in Fig. 3 and gate 15 in Fig. 4).

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murata [JP 404133154 A] in view of Shibazaki [US 5,809,257 A] as applied to claims 1, 2, 4-8, 13 and 14 above, and further in view of Gates et al. [US 5,920,708 A; hereinafter Gates].

Referring to claim 9, Murata, as modified by Shibazaki, discloses all the limitations of the claim 1 except that does not teach said connection information among said plurality of chips is composed of a packet.

Gates discloses a single pin serial port for information transfer (See Abstract and Fig. 3), wherein connection information (i.e., command byte 410 of Fig. 4B; See col. 9, lines 18-27) among a plurality of chips (i.e., LED 350, Soft Resource 360, Programmable Logic Circuit 330, Board Control Logic 370, SEEPROM 380, EEPROM 390 and Bus Terminators 360 in Fig. 3) is composed of a packet (i.e., command packet 420 of Fig. 4B).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said feature of single pin serial port with support circuit, as disclosed by Gates, in said bus selector device, as disclosed by Murata, as modified by Shibazaki, so as to communicate in a serial communication mode among said plurality of chips, for the advantage of less pins on said plurality of chips (i.e., two interconnected integrated circuits), less PCB etch routing, reduced timing constraints of multi-signal interface (viz., parallel bus interface) by elimination of signal-to-signal skew concerns (See Gates, col. 7, lines 8-13).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure.

With regard to Multiple Bus System,

Hamaguchi et al. [US 5,327,538 A] disclose method of utilizing common buses in a multiprocessor system.

Izuno et al. [US 5,717,852 A] disclose multiple bus control method and a system thereof.

Getzlaff et al. [US 5,889,969 A] disclose logical bus structure including plural physical busses for a multiprocessor system with a multi-level cache memory structure.

With regard to Bus Switching,

Nozuyama [US 5,862,359 A] discloses data transfer bus including divisional buses connectable by bus switch circuit.

Davidson [US 5,968,155 A] discloses digital gate computer bus.

Maeda [JP 406004650 A] discloses memory device.

IBM Technical Disclosure Bulletin published by IBM [September, 1987, Vol. 30, Issue No. 4, pages 1874-1875] discloses memory bus switch logic unit.

With regard to Signal Skew,

Tomita et al. [US 6,075,393 A] disclose clock synchronous semiconductor device system and semiconductor devices used with the same.

Maki [US 5,477,178 A] discloses data-hold timing adjustment circuit.

Tanaka et al. [US 5,867,541 A] disclose method and system for synchronizing data having skew.

Omori [JP 406148280 A] discloses timing skew adjusting mechanism.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Christopher E. Lee
Examiner
Art Unit 2112

cel/ CEL

Glenn A. Auve
Primary Patent Examiner
Technology Center 2100